

# *Actuating, Sensing and Control Mechatronic Systems*

## *Introduction to FPGA devices*

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Faculty of Mechanical Engineering and Robotics

AGH University of Science and Technology

## AGENDA

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### *Part I*

- 1. Course content and passing requirements*
- 2. FPGA - architecture of the system*
- 3. Comparison of MCU and FPGA*
- 4. FPGA – Ways of use*
- 5. FPGA Applications*
- 6. DE10-Lite - Development and Education Board*
- 7. Example projects implemented using FPGA*

### *Part II – Combinational circuits*

## COURSE ISSUES

### ***Motors***

- direct current motors (DC);
- stepper motors;
- linear motors;
- direct drives (BLDC, PMSM);
- synchronous motors AC;
- asynchronous motors AC;
- commutated motors AC;
- piezoelectric transducers;
- drivers and amplifiers;
- pneumatic and hydraulic actuators.

### ***Electronics***

- logic gates and flip-flops;
- combinational logic circuits design;
- sequential logic circuits design;
- microprocessors (construction and architecture);
- implementation of algorithms in FPGA;
- soft-processor Nios II.

### ***Sensors***

- sensors of non-electrical quantities (classic, MEMS);
- sensors in mechatronic systems;
- sensors as mechatronic systems.

## CONDITIONS FOR PASSING THE COURSE

Passing the course – passing grades in laboratory, project, and exam:

$$\begin{aligned} & \textit{laboratory (max 60 points)} \\ & + \\ & \textit{project (max 40 points)} \\ & + \\ & \textit{exam (motors, electronics, sensors)}. \end{aligned}$$

Passing the laboratory and the project parts - based on the number of points. Grading scale:

- (0%-49%) - **2.0**
- (50%-60%) - **3.0**
- (61%-70%) - **3.5**
- (71%-80%) - **4.0**
- (81%-90%) - **4.5**
- (91%-100%) - **5.0**

Your current points are visible on (website of Grzegorz Karpel PhD, tab Dydaktyka):

**<http://home.agh.edu.pl/~gkarpel/studenci.html>**

***A point correction in case of an excused absence.***

***Final grade:***

$$G_F = 0.35 \cdot G_{Lab} + 0.25 \cdot G_{Pro} + 0.4 \cdot G_{Exam}$$

$G_{Lab}$ ,  $G_{Pro}$  – final grades from laboratory and project;

$G_{Exam}$  – arithmetic mean from parts: motors, electronics, and sensors.

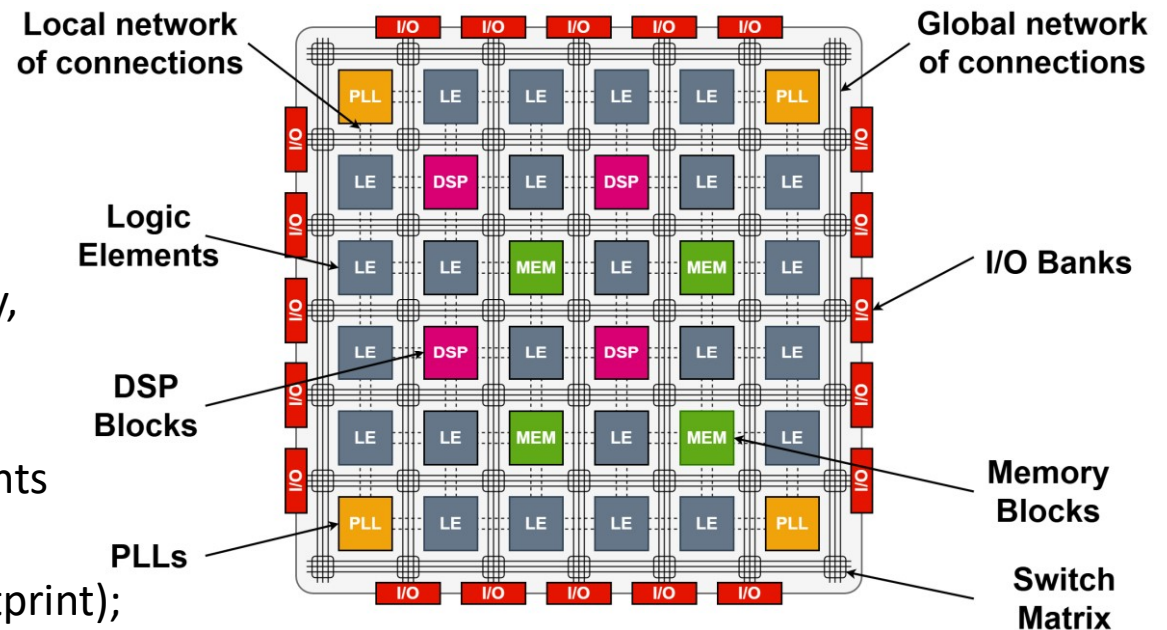
## FPGA (Field Programmable Gate Arrays)

The main components of FPGA devices:

- **LEs cells** (*Logic Elements*) / **ALM** (*Adaptive Logic Modules*) / **CLBs** (*Configurable Logic Blocks*);
- **connection network** – provides local communication with neighboring LEs and global communication within the entire FPGA chip;
- **additional elements that support implementation** (e.g. memory, multipliers, PLL loops, ADCs , etc.);
- **others** (power system, GPIO - General Input/Output Ports , etc.).

**Differences between FPGA devices  
(and devices' families):**

- number of LEs (*Logic Elements*);
- complexity level of LEs;
- device speed (maximum operating frequency, expressed as signal propagation time through LEs ~ 1-9 ns);
- the type and number of integrated equipments (memory, multipliers, PLL loops, ADCs, etc.);
- number of input/output ports (a type of footprint);
- version (commercial/industrial - depending on the operating temperature range).

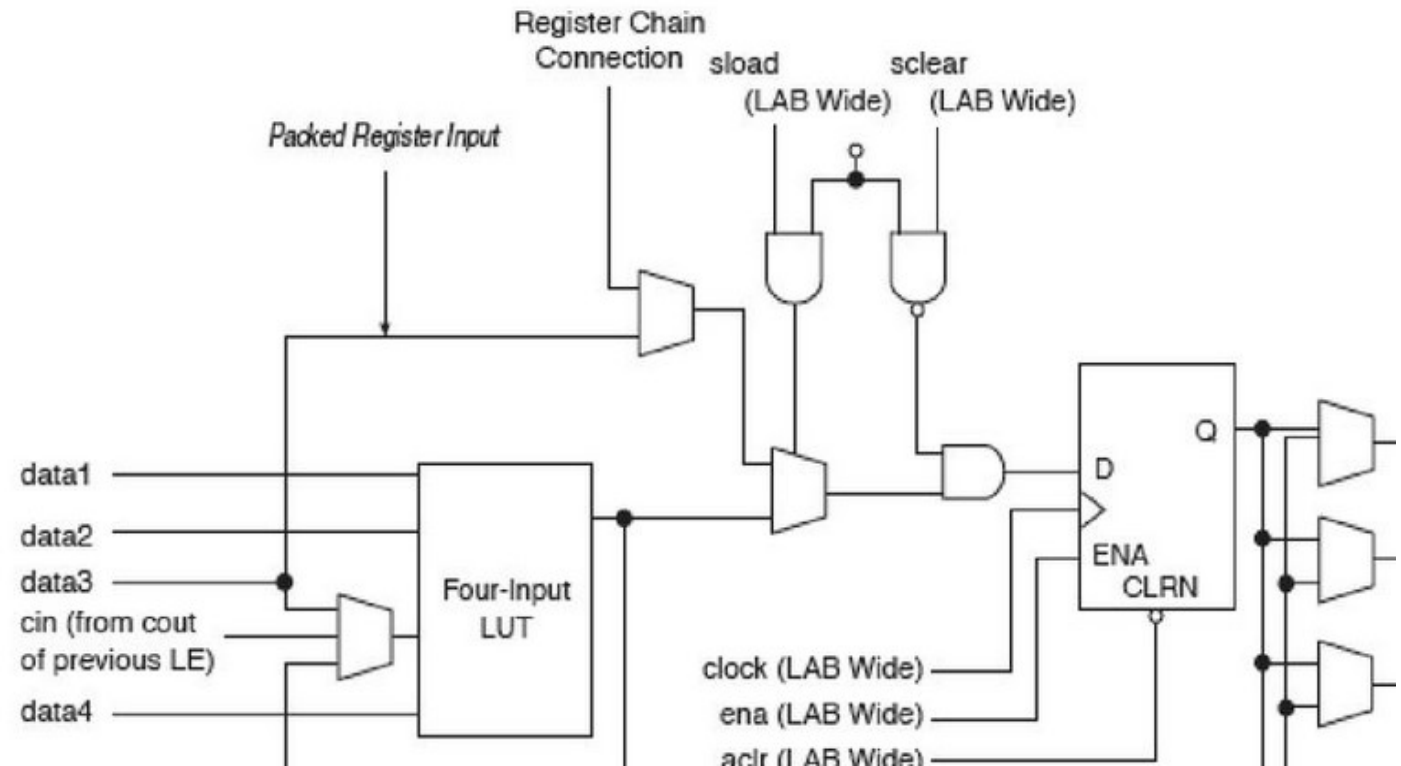


## FPGA (Field Programmable Gate Arrays)

# Altera Cyclone III Logic Element (LE) – Normal Mode

LEs cell:

- is based on a 4-bit Look Up Table (the 4 bit LUT allows to implement of any 4-bit boolean logic);
- the flip-flop allows to latch a signal (design sequential logic circuit);
- has additional elements for the internal configuration and signals multiplexing.



## FPGA vs. Microcontroller (MCU): Similarities and differences

### MCU



### FPGA



### Differences

- Fixed architecture imposed by the manufacturer
- A programming language is used as sequentially executed commands
- Multiple tasks are realized by switching between them
- Fixed, dedicated I/O ports, little possibility of changing functionality: e.g. PWM, I2C, SPI
- Built-in ADC and DAC converters

- User-configurable architecture
- A programming language is used for internal device configuration
- Tasks are realized in parallel and simultaneously
- User-configurable I/O ports, high possibility of changing a functionality
- Most often without built-in ADC and DAC converters

### Similarities

- **The digital circuit is in the form of an integrated circuit**
- **Can realize implemented algorithms/tasks**
- **Programmable by a dedicated language**

## FPGA vs. Microcontroller (MCU): Similarities and differences

**MCU**



**FPGA**



*Similarities*

- **The digital circuit is in the form of an integrated circuit**
- **Can realize implemented algorithms**  
 possibility of implementation algorithms: regulation and control systems, numerical calculations, communication with sensors and transducers by standard low-level interfaces (e.g. SPI, I2C, 1-Wire), communication with peripheral devices and systems (e.g. displays, drivers of electric motors) communication via standard interfaces (UART, Ethernet), etc.
- **Programmable by a dedicated language**  
 C / C++ / assembler – MCU;  
 VHDL / (System) Verilog – FPGA.

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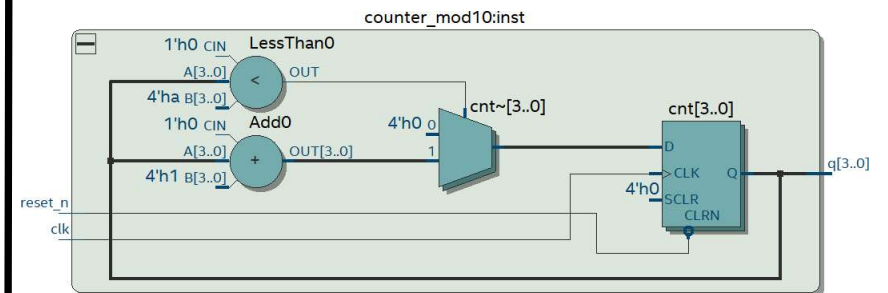
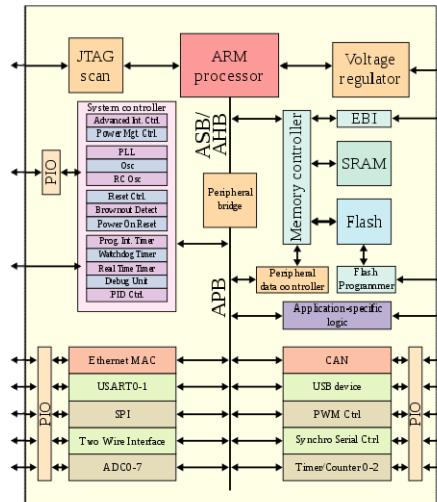
### FPGA



- Fixed architecture imposed by the manufacturer**
- + available modules/peripherals that are ready to work after simple configuration;
  - functionality limited to components built-in by the manufacturer, user cannot add or change any elements of the architecture.

- User-configurable architecture**
- + the ability to implement any module;
  - usually a longer implementation time.
- Physical architecture : LEs, connection network, etc.**
- Hardware architecture: defined by the user, e.g. mod 10 counter:**

Differences



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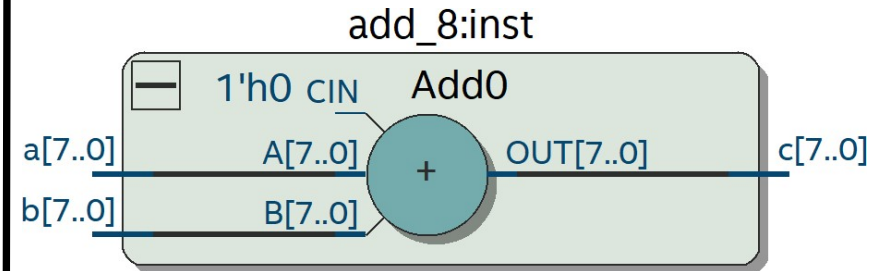
$c = a + b;$  // C language

```

edit: C:\emu8086\MySource\Sum_Two_Array.asm
file edit bookmarks assembler emulator math ascii codes help
new open examples save compile emulate calculator convertor
01 DATA SEGMENT
02 NUM1 DB 36H,55H,27H,42H
03 NUM2 DB 38H,41H,29H,39H
04 RESULT DB 5 DUP (0)
05 ENDS
06
07 CODE SEGMENT
08 ASSUME DS:DATA CS:CODE
09 START:
10 MOV AX,DATA
11 MOV DS,AX
12
13 LEA SI,NUM1
14 LEA DI,NUM2
15 LEA BX,RESULT
16
17
18 MOV CX,5
19 LOOP1: MOV AL,[SI]
20
21 ADD AL,[DI]
22 MOV [BX],AL
23
24 INC BX
25 INC SI
26 INC DI
27
28 LOOP LOOP1
29
30 MOV AH,4CH
31 INT 21H
32 ENDS
33 END START
34
35
line: 27 col: 33 drag a file
  
```

A programming language is used for internal device configuration

$c \leq a + b;$  // VHDL language



Differences

## FPGA vs. Microcontroller (MCU): Similarities and differences

**MCU**



**FPGA**



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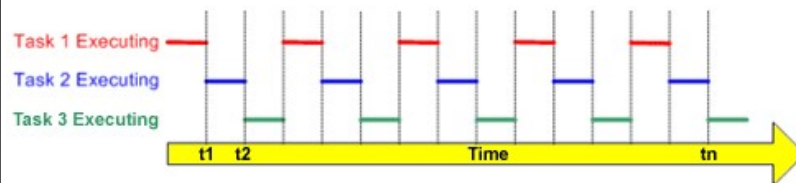


### FPGA



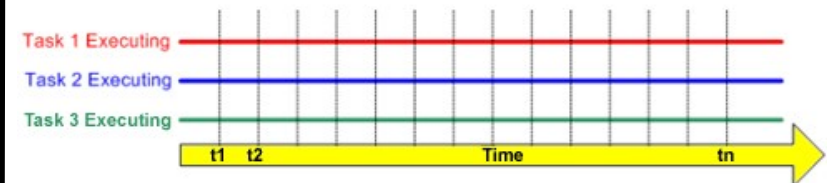
Multiple tasks are realized by switching between them

- each task is allocated a specific time slot;
- increasing the number of tasks has an impact on the handling time of the other tasks;
- it is usually necessary to assign priorities to tasks;
- some problems in real-time systems with maintaining a constant and high frequency of operations.



Tasks are realized in parallel and simultaneously

- a different part of the hardware is responsible for each task;
- adding a new task does not affect the other tasks;
- the only consequence of adding a new task is the use of additional FPGA resources;
- often, the user has the ability to optimize algorithms in terms of speed (operating frequency) or hardware resources.



Differences

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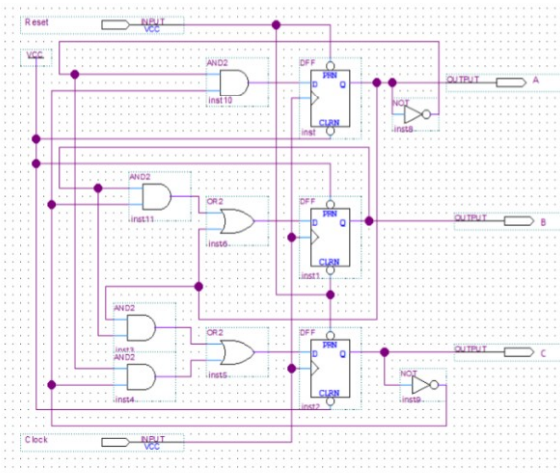
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## FPGA – Ways of use

### Block schematic

- Basic logic elements  
(e.g. logic gates, flip-flops)
- Hardware blocks generated by the auxiliary tools  
(e.g. counters, multiplexers)
- Custom hardware blocks  
(implemented in HDL by the user)



### HDL (Hardware Description Languages)

The most commonly used:

- VHDL
- (System) Verilog
- System C

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4
5 entity signed_adder is
6   port
7   (
8     aclr : in  std_logic;
9     clk  : in  std_logic;
10    a    : in  std_logic_vector;
11    b    : in  std_logic_vector;
12    q    : out std_logic_vector
13  );
14 end signed_adder;
15
16 architecture signed_adder_arch of signed_adder is
17   signal q_s : signed(a'high+1 downto 0); -- extra bit wide
18
19 begin -- architecture
20   assert(a'length >= b'length)
21     report "Port A must be the longer vector if different sizes!"
22     severity FAILURE;
23   q <= std_logic_vector(q_s);
24
25   adding_proc:
26   process (aclr, clk)
27     begin
28       if (aclr = '1') then
29         q_s <= (others => '0');
30       elsif rising_edge(clk) then
31         q_s <= ('0'&signed(a)) + ('0'&signed(b));
32       end if; -- clk'd
33     end process;
34
35 end signed_adder_arch;

```

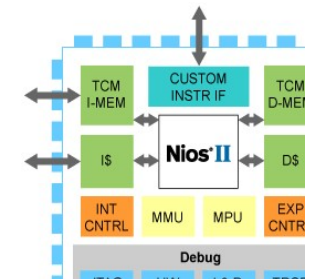
### Soft-processor (e.g. Nios II)

Advantages :

- user-configurable architecture;
- possibility of implementation your own peripherals;
- the ability to divide tasks into hardware and software parts;
- possibility of implementation several S-P units in one integrated circuit.

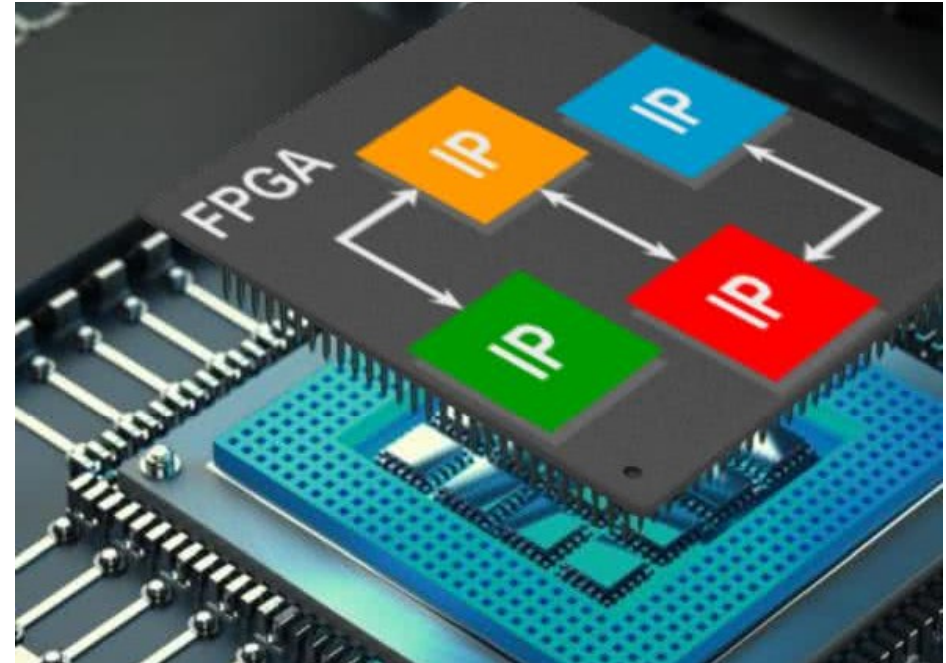
Disadvantages :

- lower operating frequency  
(clock speed);
- usually this platform is more expensive.



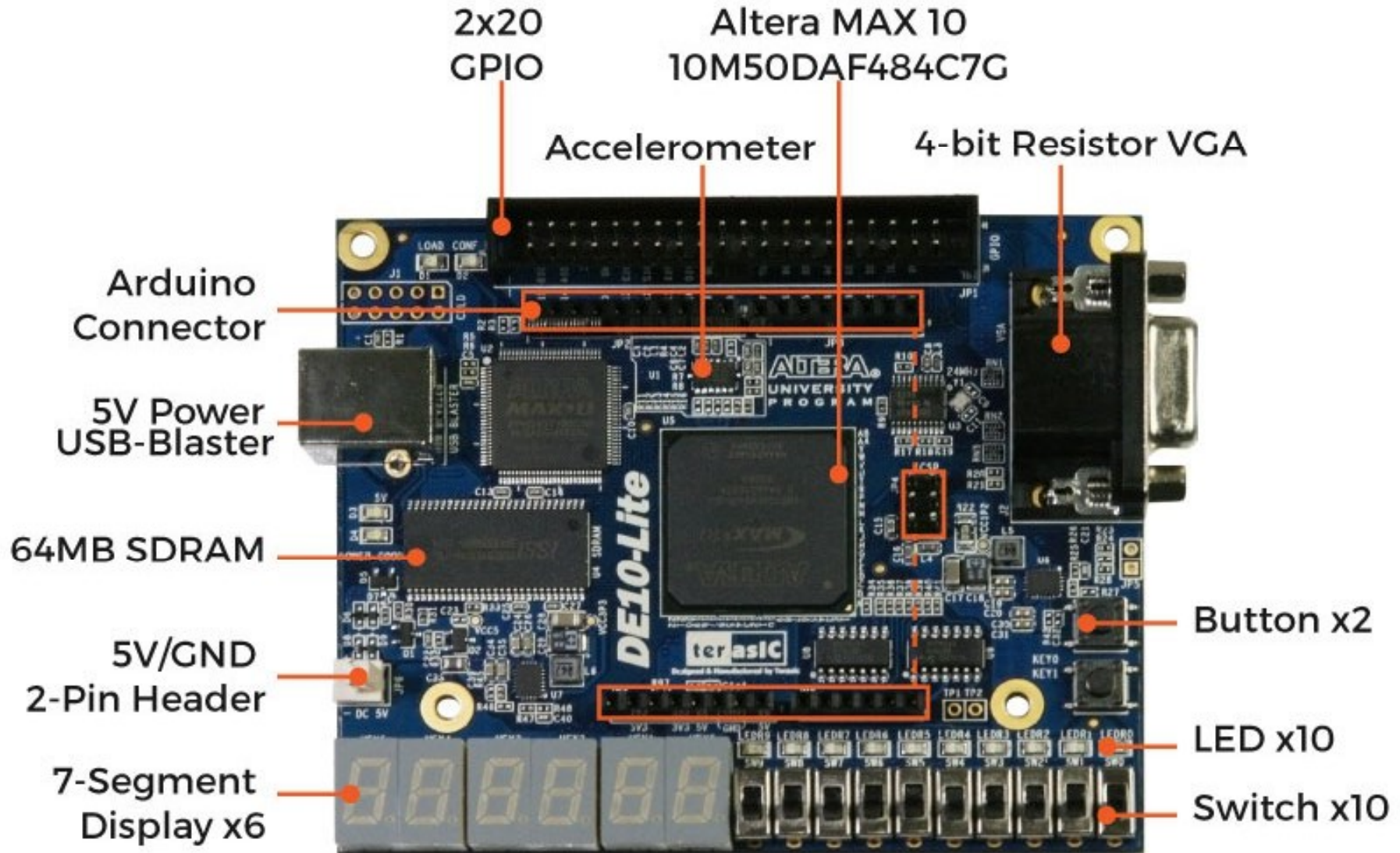
## FPGA Application

- Embedded systems
- Measurement cards
- Military applications
- Network applications
- Power electronics
- Control systems of mechatronic devices
- Implementation of numerical computations
- Digital Signal Processing (DSP)
- Image processing systems
- ASIC prototyping





## DE10-Lite Development and Education Board



## BIBLIOGRAPHY

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- [1] <https://www.intel.com/>
- [2] <https://www.terasic.com.tw/en/>
- [3] <https://kamami.pl/>
- [4] <https://www.arm.com/>
- [5] <https://allaboutfpga.com/>

### Video

- [A] [https://www.youtube.com/watch?v=G-dKPe4Zz\\_M](https://www.youtube.com/watch?v=G-dKPe4Zz_M)
- [B] <https://www.youtube.com/watch?v=CnSE-gF4jng>
- [C] <https://www.youtube.com/watch?v=IG2I56NKLQk>
- [D] [https://www.youtube.com/watch?v=k\\_7IV0U2JhQ](https://www.youtube.com/watch?v=k_7IV0U2JhQ)
- [E] [https://www.youtube.com/watch?v=CXb\\_m8p3Yt4](https://www.youtube.com/watch?v=CXb_m8p3Yt4)
- [F] <https://www.youtube.com/watch?v=ANxHyCAYGp0>
- [G] <https://www.youtube.com/watch?v=NBtGxF4UZRs>