Counters

Requirements for the exercise (issues and skills necessary to complete the task):

- representation of numbers in decimal, binary and hexadecimal systems;
- setting up a new project in Quartus Prime;
- creating a hardware module (symbol) in Quartus Prime based on a schematic file (*.bdf);
- creating a hardware module (symbol) in Quartus Prime based on a source code file (eg. *.vhd);
- ability to simplify a logical expressions using the Karnaugh Map method;
- ability to implement a scheme with logic gates based on an algebraic equation;
- **knowledge of the excitation tables of the flip-flops: D, T, JK;**
- **ability to synthesize synchronous logic circuits**

Agenda:

1. Designing an example counter mod 5/6/7 counting up/down, based on the T flip-flop.
2. Implementation of the example counter on an FPGA device:
    a. implementation of counter ***(0.5 p.)***;
    b. implementation as hardware block (created symbol file) ***(0.25 p.)***;
    c. displayed value on 7-segment display ***(0.25 p.)***;

/* Proceed to the next part after presenting the results to the teacher */

3. Individual task for each team: design and implement counter according to the task (mod 4/5/6/7/8 synchronous up/down counter, based on D/T flip-flop) ***(0.5 p.)***:
    a. design and implement a counter;
    b. implementation as hardware block – symbol file;
    c. displayed value on 7-segment display;

    /* Proceed to the next part after presenting the results to the teacher */

    d. adding an input controlling the counting direction – dir ***(0.25 p.)***;
    e. adding an input controlling start/stop – enable ***(0.25 p.)***:
        - as counter input;
        - by clock gating.

In order to test the counter use ***MultiPrescaler*** and seven segment display controller, as in the figure below (Fig. 1).